NEURAL IMPLANTS, PACKAGING FOR BIOCOMPATIBLE IMPLANTS, AND IMPROVING FABRICATED CAPACITORS

A Thesis

Presented to the Faculty of the Graduate School

of Cornell University

In Partial Fulfillment of the Requirements for the Degree of

Master of Science in Electrical and Computer Engineering

by

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ABSTRACT

We have completed the circuit design and packaging procedure for an NIH-funded neural implant, called a MOTE (Microscale Optoelectronically Transduced Electrode). Neural recording implants for mice have greatly advanced neuroscience, but they are often damaging and limited in their recording location. This project will result in free-floating implants that cause less damage, provide rapid electronic recording, and increase range of recording across the cortex. A low-power silicon IC containing amplification and digitization sub-circuits is powered by a dual-function gallium arsenide photovoltaic and LED. Through thin film deposition, photolithography, and chemical and physical etching, the Molnar Group and the McEuen Group (Applied and Engineering Physics department) will package the IC and LED into a biocompatible implant approximately $100\mu m^3$. The IC and LED are complete and we have begun refining this packaging procedure in the Cornell NanoScale Science & Technology Facility.

ICs with 3D time-resolved imaging capabilities can image microorganisms and other biological samples given proper packaging. A portable, flat, easily manufactured package would enable scientists to place biological samples on slides directly above the Molnar group's imaging chip. We have developed a packaging procedure using laser cutting, photolithography, epoxies, and metal deposition. Using a flip-chip method, we verified the process by aligning and adhering a sample chip to a holder wafer.

In the CNF, we have worked on a long-term metal-insulator-metal (MIM) capacitor characterization project. Former Fellow and continuing CNF user Kwame Amponsah developed the original procedure for the capacitor fabrication, and another former fellow, Jonilyn Longenecker, revised the procedure and began the arduous process of characterization. MIM

caps are useful to clean room users as testing devices to verify electronic characteristics of their active circuitry. This project's objective is to determine differences in current-voltage (IV) and capacitor-voltage (CV) relationships across variations in capacitor size and dielectric type. This effort requires an approximately 20-step process repeated for two-to-six varieties (dependent on temperature and thermal versus plasma options) of the following dielectrics: HfO2, SiO2, Al2O3, TaOx, and TiO2.

BIOGRAPHICAL SKETCH

Before Cornell, Rose completed two bachelor's degrees: a B.A. in Neuroscience and Film Studies at Wesleyan University (2010), and a B.S. in Electrical and Computer Engineering at the University of Maryland, College Park (2013). She made the seemingly strange transition because she decided she wanted to create electronic devices to improve and accelerate neuroscience research. In August 2013, she joined the Molnar Group at Cornell, which develops electronic neural interfaces as well as imagers and RF integrated circuits (ICs). Rose's research interests include CMOS circuit design and packaging for neural recording and imaging devices.

In addition to her research pursuits, Rose is involved with many groups committed to outreach and improving the graduate community. As the Director of the Graduate Society for Women Engineers at Cornell, she coordinates outreach events to promote STEM careers among local youth, organizes professional development talks for graduate engineers, and runs social activities to engage and support diverse graduate engineers. She also participates in STEM outreach as a CNF Outreach Ambassador and a volunteer with Destination Imagination. Rose is a founding member of the Graduate and Professional Students for Sexual Violence Prevention, which designs consent and bystander programming that targets graduate students in all departments.

Dedicated to Nicolas François Mendoza

Because he dedicated his thesis to me.

ACKNOWLEDGMENTS

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CHAPTER 1
NEURAL MOTE IMPLANTS: INTRODUCTION

Introduction and Goals

We know very little about the brain, but as electrical engineers, we can strive to design innovative electronics to facilitate neuroscientific discovery. Much of what we know about the brain consists of links between form (brain regions) and function (purpose in controlling behavior). For example, areas of the medial temporal lobe are associated with long-term memory formation and storage, and the prefrontal cortex is associated with planning, inhibition, and social behavior. Tools such as MRI, fMRI, PET, and ECoG have enabled such discoveries, but these do not enable study of neural circuitry in precise anatomic regions. Neural implants, however, do.

With their precision and penetrative capabilities, neural probes are implants that can investigate lab mammal microcircuitry over weeks- to months-long periods. Since the first cochlear implant by Djourno and Eyriès in 1957 neuroscientists have used probes in revolutionary studies such as the discovery of hippocampal place cells (1, 2). Serious damage to the lab animals from probes occurs even with innovative flexible probes (3)

Optical probes incorporate the nascent field of optogenetics to stimulate neural tissue using waveguides. This probe type can target individual cells and specific cell types (e.g. excitatory glutamatergic motor cortex neurons). In early optogenetic experiments, Diesseroth achieved whisker motor control in rats and mice (4). However, state-of-the-art optogenetic probes are millimeters long, even when researchers achieve exceptionally thin widths (e.g. 150μm) and thicknesses (50μm) (5). Even when optical probes have a thin design, their length and stiffness is highly damaging to brain tissue, suitable only for acute experimentation.

Free-floating implants cause less damage than probes and can rapidly record spiking from a greater array due to coupling and distribution. Because they are untethered upon insertion into neural tissue, free-floating implants move with the brain's movement during normal behavior, reducing shearing damage. However, the latest implants have dimensions of several hundred microns, or alternatively require multiple components, such as an external transceiver and a sub-dural transceiver, in addition to the "neural dust" (6, 7). Additionally, these efforts have not achieved implant functionality at depths greater than 2mm (7). No publications include information on tissue damage from free-floating implants.

Our free-floating, dispersed implant project combines the scalability of other neural dust implants but requires no transceiver components, is wireless, minimizes size, and has the potential for deeper implantation. Our MOTEs (Microscale Optoelectronically Transduced Electrodes) will detect and encode local extracellular neural signals. One or more light sources will provide power to the MOTEs, and they in turn will emit light-pulse representations of their digital output signals. In the ideal, ultimate manifestation of our project, a physician will implant multiple MOTEs into the cortex of a patient, and will periodically monitor neural function in specific brain regions in addition to synchronicity of spiking across regions (perhaps indicating epileptic seizures).

Each letter of the MOTE acronym refers to an essential aspect of our project. The MOTE is microscale—specifically, our ideal size is $50\mu m^3$—because we want to limit gliosis. Additionally, researchers found that minimizing MOTE dimension and power supply while maintaining signal-to-noise ratio offers scaling down to 50μm (8). We achieve this small scale using integrated circuits in a CMOS (complementary metal-oxide-semiconductor) technology. Optoelectronic describes the method of power and transmitting information from the MOTE.

Light inputs from a laser bean causes a voltage across the photovoltaic devices, and current through the output LEDs cause light pulse emission. The light—comprised of photons—is transduced to electricity—comprised of electrons—to power the MOTE and back again as output light flashes. Finally, the MOTE contains electrodes, described below.

The MOTE device consists of platinum-coated electrodes, gallium arsenide (GaAs) LEDs, and integrated circuits. We create the preliminary electrodes by layering stacks of metal layers over each input pin in the Cadence layout for the circuit (see Chapters 2 and 4 for information about circuitry). As part of the packaging procedure, we will coat the two metal stacks with platinum to complete the biocompatible electrode. These electrodes detect extracellular neural signals via changes in the electric field around a cell. Extracellularly, current generally flows from dendritic "sources" to somatic "sinks." We will use platinum because, compared to tungsten, iridium, or other biocompatible metals, platinum helps minimize electrode noise. Metal extracellular electrodes function as capacitors with an impedance inversely proportional to the frequency of the applied signal (9).

The GaAs devices in our MOTE will serve as both photovoltaic power devices and LED output transmitters. The GaAs LEDs consist of seven layers: a GaAs wafer (check) layer, an AlGaAs stop layer, a p-doped GaAs layer, two p-doped AlGaAs layers, an n-doped AlGaAs layer, and finally an n+ GaAs layer. The recombination of holes and electrons between the n and p layers causes the characteristic photon release. We use metal organic chemical vapor deposition (MOCVD) to form the differently-doped layers of GaAs and AlGaAs. This stacked structure requires several clean room procedures in order to create bondable LEDs.

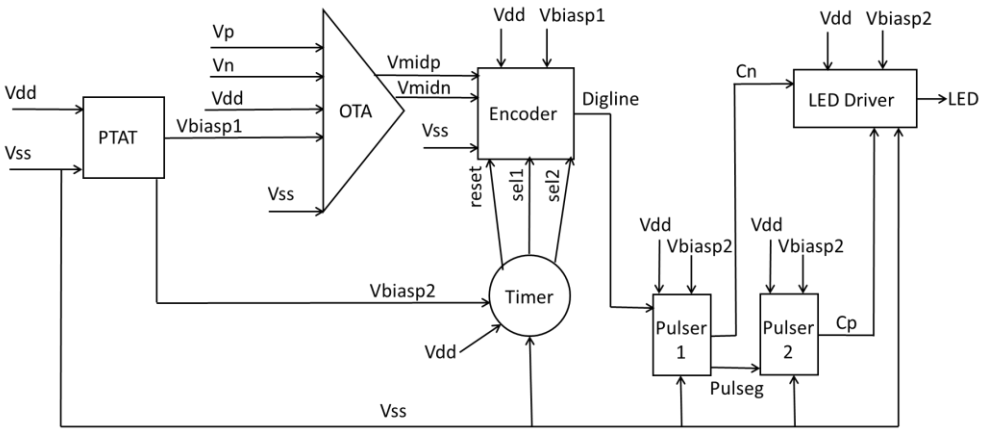
There are four basic steps to the LED release process. First, we must flip upside-down the LED structure described above. Then, we deposit Al2O3 dielectric insulation via atomic layer

deposition (ALD) on a Si wafer, and wafer-bond the LED structure to it. We wet etch the top GaAs layer at the top of the LED structure to expose the stop layer. Afterwards, we remove the stop layer using HF to expose the first p-type GaAs layer. Finally, we use a mask and citric acid to etch through the top four remaining LED layers to expose part of the n+ type GaAs layer. The n+ GaAs layer provides an adhesion and insulation layer, enabling an appropriate surface for metal evaporation to create pads.

System Overview for 130nm BiCMOS

The 130nm BiCMOS version of the MOTE consists of seven sub-circuits and five input/output signals. Externally produced power (Vdd) and ground (Vss) feed into the first circuit, the PTAT (Proportional to Absolute Temperature) circuit, which produces voltage bias signals for subsequent circuits. Next, the OTA (Operational Transconductance Amplifier) amplifies and filters input neural signals from the positive and negative electrodes. The Encoder includes a second amplifier stage and produces a digital signal at a frequency determined by the Timer circuit. Two identical Pulser circuits take in the digital output of the encoder and produce non-overlapping pulse signals that control the switching mechanism of the LED Driver, which produces current pulses to drive the LEDs.

FIGURE 1: System Diagram of 130nm BiCMOS Chip

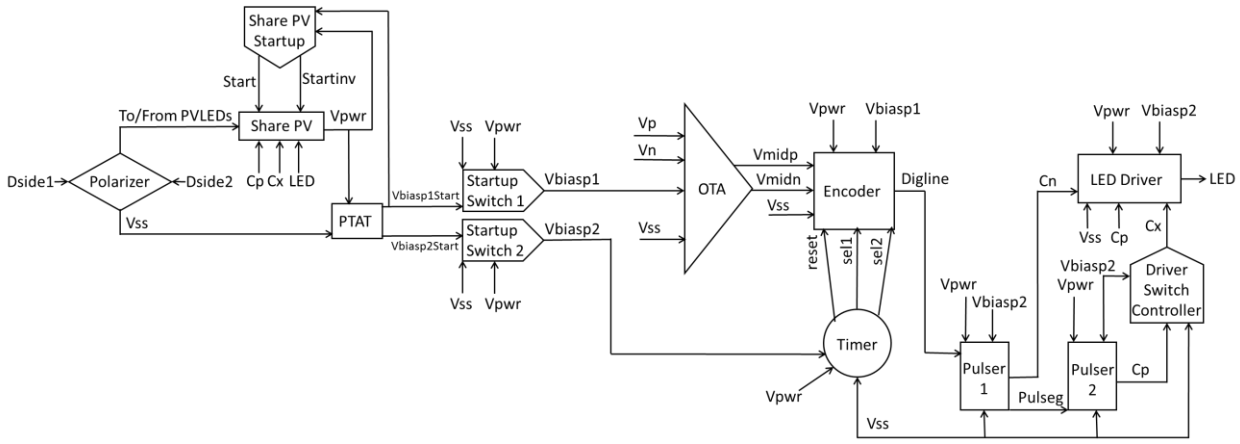


System Overview for 180nm Low-Voltage

Unlike the 130nm version, the 180nm version includes does not assume power and ground supplies are identified and separated off-chip; we have created a high-versus-low initial switch, the Polarizer, to free the researcher from needing to properly orient the LED when bonding the MOTE and LED. This switch is one of thirteen sub-circuits of this version of MOTE, which has only four input/output signals. The two input/output signals, Dside1 and Dside2 (‘D’ for diode), are the two signals from either side of the GaAs LED. After the Polarizer determines the correct high versus low orientation of the LED signals, it emits the two signals as To/From PVLEDs and Vss. The start-up circuitry also includes Share PV, Share PV Startup, and two Startup Switches.

Like the 130nm version of MOTE, the 180nm IC includes a PTAT, an OTA, a Timer, an Encoder, two Pulsers, and an LED Driver, but the 180nm version additionally includes a Driver Switch Controller to produce an additional control signal for improved LED Driver function.

FIGURE 2: System Diagram of 180nm Low-Voltage Chip

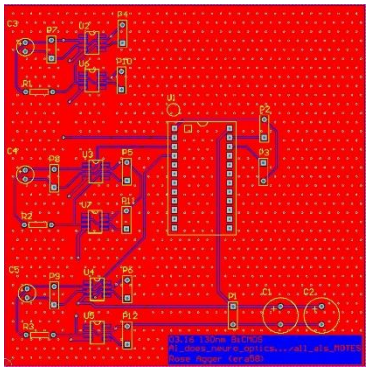


Testing Setup

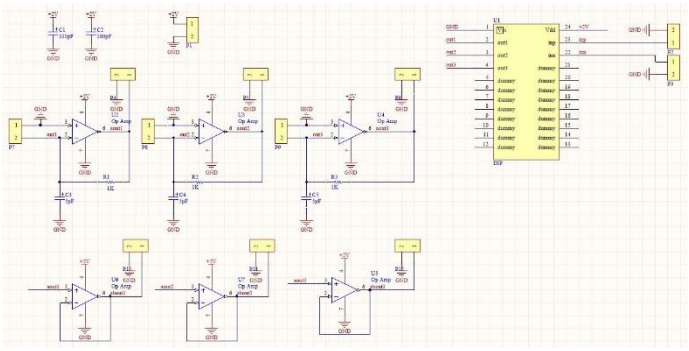
Testing the 130nm chip involved connection via PCB to multiple power and measurement instruments. The PCB contains transimpedance amplifiers to amplify and convert the output current signal from the LED Driver to a voltage, and voltage buffers to isolate this voltage output from the IC's output. The transimpedance amplifier contains a resistor to set the gain according to Equation 1, and a capacitor to include low-pass filtration to the feedback path. Additionally, two large capacitors between Vdd and Gnd provide decoupling.

EQUATION 1: $$V_{out} = I_{in}R_f$$

FIGURE 3: (a) PCB Schematic, (b) Layout



(a) PCB schematic shows coupling capacitors and header pin for power and ground at top left, symbol for IC package at top right, three transimpedance amplifiers in middle row, and three voltage buffers at bottom.



(b) Top layer of PCB layout shows amplifiers on left, IC package footprint in the middle, and capacitors and power/ground header at bottom left.

To power and ground the PCB set-up, we used a single chafnnel voltage source, Keithley 2400 SourceMeter. We connected a function generator, Tektronix AFG3102C Dual Channel Arbitrary/Function Generator, to test the IC using a variety of sinusoidal signals to represent the positive and negative input signals. We varied both amplitude and frequency of the signals within a large, semi-realistic range (amplitude 100uV to 1mV and frequency 300Hz to 10kHz). Lastly, we used a Tektronix TDS 2014B Four Channel Digital Storage Oscilloscope to check proper connection of signals, signal degradation, and outputs.

Because we had trouble analyzing the gigahertz-range output signals (discussed in the next chapter), we also used a National Instruments (NI) Data Acquisition system (DAQ). We connected the output signal to an SCB-68A Data Acquisition kit, which fed into an NI PXIe-6368 card in an NI PXIe-1071 chassis. The chassis also contained an NI PXIe-8375 card, which interfaced with a Dell Optiplex 7020 computer via an internal SHC68 card. We used the NI MAX software to establish proper linkage, and MATLAB to record and analyze data (see Chapter 3).

CHAPTER 2

NEURAL MOTE IMPLANTS: 130NM BICMOS CIRCUITRY

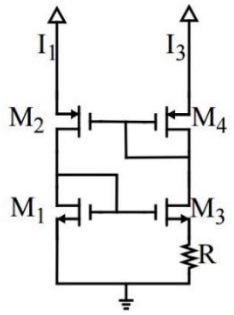
PTAT

The PTAT provides a stable current regardless of Vdd level. The standard choice for producing voltage and current bias sources is a series of current mirrors, but these are dependent on Vdd. We care about Vdd-independent biases because we want the MOTEs to function over a range of voltages provided by the photovoltaic configuration of the LEDs. Ideally, the MOTEs should function over a Vdd range of 700mV to 1.5V.

Our PTAT provides two bias currents, Vbiasp1 and Vbiasp2. Two currents are necessary because this helps isolate noisier sub-circuits from less noisy sub-circuits. As seen in Figure 1, the OTA and the Encoder both use Vbiasp1, while the remaining sub-circuits use Vbiasp2. We predicted that these sub-circuits experience more jitter and contribute significantly more noise than the others, so they make Vbiasp1 less stable than Vbiasp2.

To create a constant current, PTAT reference circuits use a cascode, current mirrors, and a reference resistor. Figure 4 shows a traditional CMOS PTAT (10). In this figure, pfets (p-channel MOSFETs) M2 and M4 act as a current mirror, so the same amount of current runs through both branches. These two transistors are in strong inversion, and nfets (n-channel MOSFETs) M1 and M3 are in weak inversion. The resistor R forces the source of M3 to stay at a set voltage, which depends on thermal voltage, electron mobility, oxide capacitance, and transistor sizing, as in equation 2.

Figure 4: CMOS PTAT



Schematic of CMOS PTAT current source with reference resistor.

Equation 2: $$V_R = U_T \ln\left(\frac{\beta_3\beta_2}{\beta_1\beta_4}\right),\ U_T = \frac{kT}{q},\ \beta_n = \mu_n C_{ox}\left(\frac{W}{L}\right)_n$$

In the case of our PTAT, all of the transistors are in subthreshold saturation, which changes the relationship between bias current and reference resistor value. For subthreshold MOSFETs, Equation 3 applies, so solving for the bias current I_{ref} with respect to reference resistor R_{ref}, we find the results shown in Equation 4, where N is the square root of the ratio of the size of transistor M3 to the other (identically-sized) transistors. However, subthreshold saturation changes the fundamental current-voltage relationships of transistors, so we find a slightly different relationship between I_{ref} and R_{ref}, as in Equation 5 (see Appendix 1).

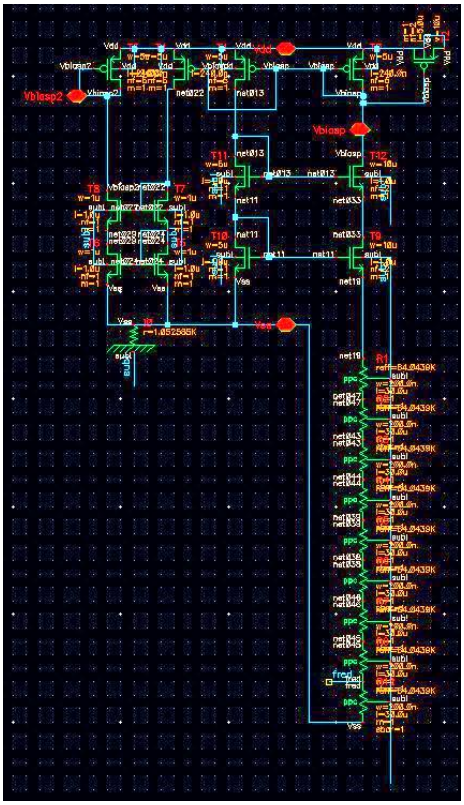
Equation 3: $$g_m = {I_D}/{U_T}$$

Equation 4: $$I_{ref} = \frac{U_T \ln(N)}{R_{ref}}$$

Equation 5: $$I_{ref} = \frac{U_T \ln N}{\kappa R_{ref}},\ \kappa = \frac{C_{ox}}{C_{ox} + C_{dep}} \approx 0.7$$

Our PTAT circuit creates a bias current through the two leftmost branches using cascodes, and the Vbiasp1 current (let us call it I_{ref1}) mirrors over to the T1 and T0 branches (Figure 5). Pfet T2 functions as a moscap (MOS capacitor), which adds a small current to I_{ref1}, and decouples Vbiasp1 from Vdd. We needed a high value resistor to create low current bias levels, so the resistor size versus the power consumption of the PTAT became an area of concern during our circuit design.

Figure 5: Schematic of BiCMOS 130nm PTAT



PTAT: Size versus Function

The primary tradeoff for the PTAT circuit is its size on the taped-out IC versus its functionality in biasing other sub-circuits. Nine P+ poly OP 64.0439kOhm resistors, totaling 576.395kOhms, make up the PTAT resistor. These resistors account for 49.94% of the entire PTAT layout and four percent of the entire functional layout of the 130nm MOTE (minus the pads). We determined from circuit simulation that the OTA remains functional (amplifies neural

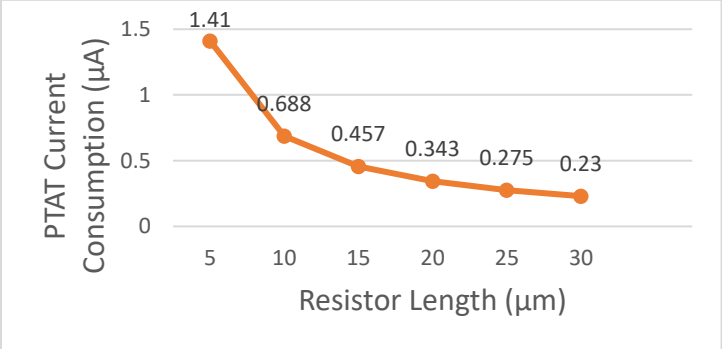
signal, gain over 29dB) when the total resistor size is decreased by a factor of six (via decreasing resistor length).

The power consumption of the PTAT is directly proportional to the size of the PTAT. Although PTATs should provide constant current sources independent of Vdd, this was not the case for our PTAT. According to our calculation for the relationship between the resistance value and size of the P+ poly OP resistors in Equation 6, we find the relationship in Equation 7. These results do not match our simulation (Figure 6), however this could be due to simplifications in the formula and the effects of a completely subthreshold saturation PTAT.

Equation 6: $R_{nom} = \left(R_S \times \frac{L}{W}\right) + \left(2 \times \frac{R_{end}}{W}\right)$

Equation 7: $P_{PTAT} = IV = \frac{W \times V_{dd} U_T \ln N}{L \times 0.2206 \kappa R_S}$

Figure 6: Effect of Varying PTAT Resistor Size on PTAT Current Consumption



OTA

The OTA amplifies, filters, and increases the robustness of the input neural signals. These functions are important to the overall MOTE because the input neural signals can be noisy, and their amplitude can range from 10uV to 1mV. Simply, in order to maintain proper MOTE

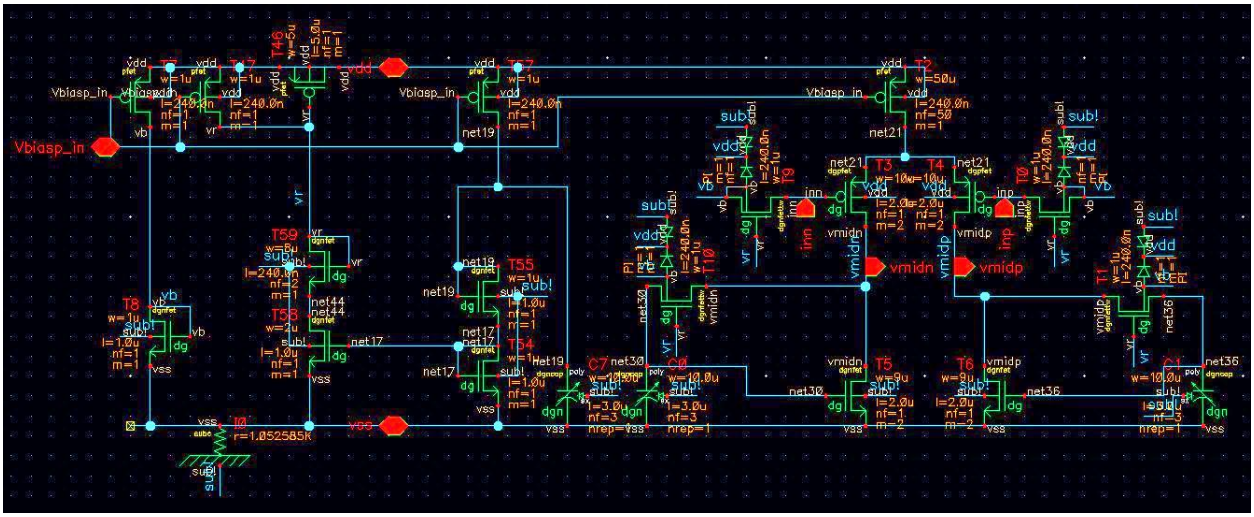
function for a variety of inputs, we need gain, filtering, and linearity. The OTA is a one-stage band-pass amplifier with start-up circuitry.

The OTA uses bias voltage Vbiasp1 (and therefore I_{ref1}) to decouple the low-frequency swing caused by the neural input. Looking at Figure 7 and proceeding left to right through the circuit, we incorporated biasing, start-up, and more biasing ahead of the amplifying stage. Voltage Vb sets the DC bias voltage level for the inputs to the amplifier, Vn and Vp. This mid-range DC bias signal is important for the neural input signals because they may be floating and AC-only.

Vr is a start-up voltage signal. Before we provide power to the IC, Vdd is low, and therefore Vbiasp1 is initially low. The pfet T17, the second-from-top-left pfet, is 'on' initially since its gate voltage, Vbiasp1, is low. This pfet charges up the moscap to its right, T46, which pulls up signal Vr. Check what follows here. Then, the current through the second-to-left branch (the Vr branch) is mirrored to the third-from-left branch. The resulting voltage change charges up the dgn (dual-gate n-type) capacitor C7, which enforces a current limit into the amplifier through pfet T2. Note that dual-gate nfets and pfets are used throughout much of the OTA because in simulation, they separate the input signal and gain control across over two gates, increasing small-signal stability (compared to single-gate MOSFETs). Physically, dual-gate MOSFETs improve isolation with a thicker gate oxide layer.

The input differential pair of dgpfets (dual-gate pfets) are placed in a triple-well configuration to reduce signal and noise coupling. Our triple wells create a buffer (a deep n-well) between the active components in the p-well and the noisy p-substrate. Below the differential pair, we have designed feedback circuitry that suppresses DC offset at high frequencies. At low frequencies, however, the loop functions as a diode-connected nfet.

Figure 7: Schematic of BiCMOS 130nm OTA



OTA: Noise versus Power

For the OTA, we have calculated and measured a trade-off between noise and power. In Equation 8, we see that the output noise for a common drain amplifier is inversely proportional to g_m, or the transconductance of the amp. For differential pair amplifiers like our OTA, however, noise currents from each device split, divide, and cancel out such that Equation 9 results, wherein the output noise is directly proportional to g_m. We can extrapolate from this and Equation 10 that increasing OTA power will also increase noise. To prove this, we found a relationship between the bias current and the total current into the OTA, and found Equation 11, which further proves that more power means more noise.

Equation 8: $$\overline{V_{n,in}^2} = \frac{4kT\gamma}{g_m} + \frac{\kappa}{WLf}$$

Equation 9: $$\overline{v_{od}^2} = \left(\overline{i_{d2}^2} + \overline{i_{d1}^2}\right) = 2\left(4kT\gamma g_m + \frac{K_{fl} I_{bias}}{2L^2 f}\right)$$

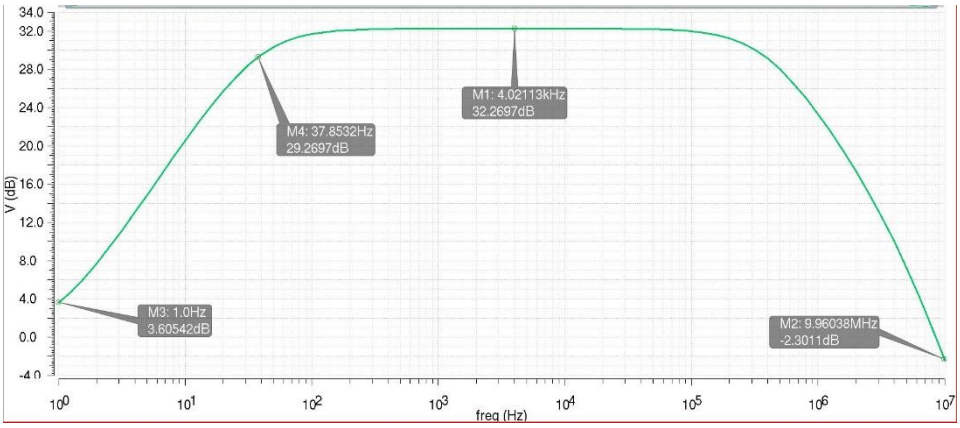
Equation 10: $$g_m = {}^{2I_D}/_{V_{OV}} = {}^{2(I_{bias}/2)}/_{V_{OV}} = {}^{I_{bias}}/_{V_{OV}}$$

Equation 11: $$P = IV = \frac{1.62L^2 f\left(\overline{v_{od}^2} - 8kT\gamma g_m\right)}{K_{fl}}$$

We found from our noise analysis that the thermal noise dominates the total OTA noise, and as expected, the diff pair is the largest contributor of noise (70%). The other transistors that contributed to the bulk of the noise were the four nfets in the feedback pathway below the diff pair (see Figure 6, dgnfets 1, 10, 5, and 6). The total summarized noise for the OTA is 367.73µV.

An AC analysis of the OTA (including the amplifying stage of the encoder) shows that the gain is 32.3dB. The bandwidth for this maximum gain is about 100Hz to 10kHz. The -3dB points are 37.85Hz and 387.8kHz (see Figure 8).

Figure 8: AC Analysis of OTA with Amplifying Stage of Encoder

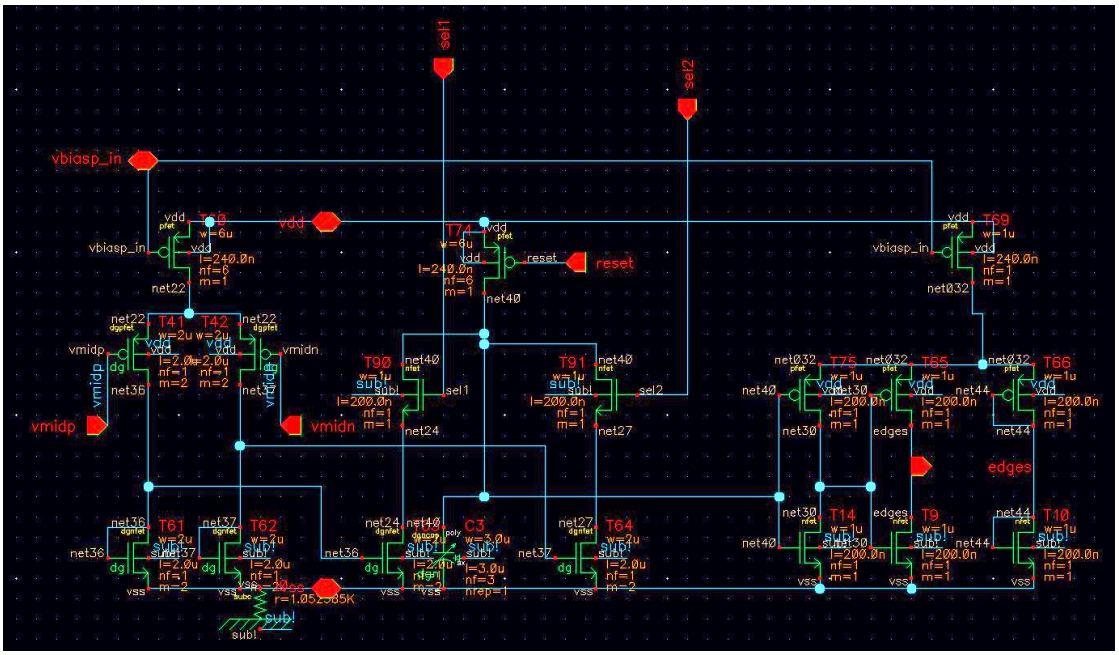


Encoder

The sub-circuits within the encoder include, from left to right: an amplifier, nfet switching circuitry, and an inverting and buffering stage (Figure 9). The bottom-most nfets to the right of the amplifier are switched on during peaks in the output of the amplifier. Therefore, these two nfets (T63 and T64) alternate between which is on and which is off. T63 and the nfet above it, T90, work together. When sel1 and the output from the Vmidp side of the amplifier are both high, capacitor C3 charges up. T64 and T91 work together in the same way, but for the Vmidn side output. The reset signal from the Timer circuit keeps pfet T74 off unless either sel1 or sel2 is switching high. When the reset pfet is on, it pulls the digital line signal high. The

double-inverter structure serves as a voltage buffer so the signal from the reset/select structure is definitively high or low at the output of the encoder.

Figure 9: Schematic of BiCMOS 130nm Encoder

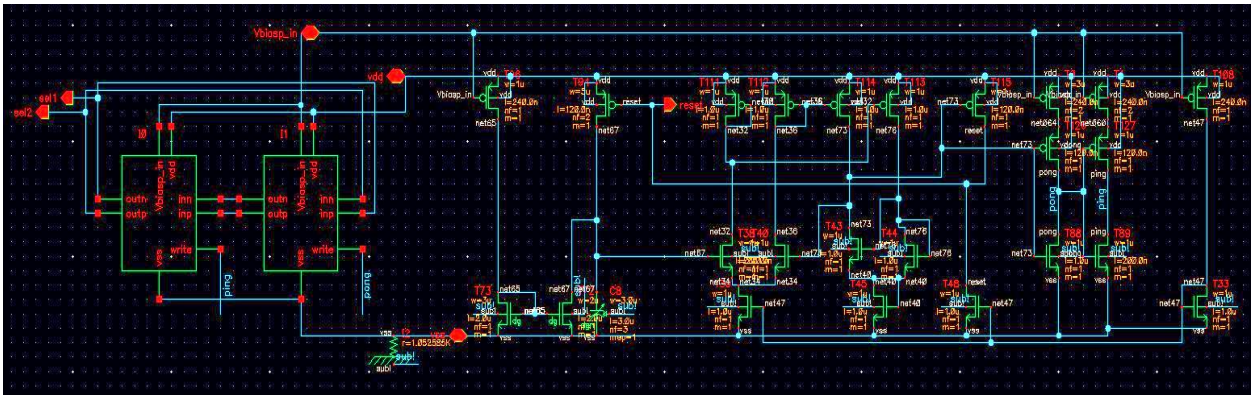


Timer

Two latches in feedback generate sel1 and sel2, opposite-sign square pulse signals with 50% duty cycle at approximately 20kHz (Figure 10). The ping/pong circuitry on the right side are opposite-sign, skinny square pulses at twice the frequency of sel1 and sel2 (about 40kHz). Inside the two latches, the opposite-sign input square pulse signals alternately turn either the left or the right nfet on, which either pulls the input of the left inverter and the output of the right inverter down, or pulls the output of the left inverter and the input of the right inverter down. This feedback loop within each latch acts as a buffer to produce the output. The two latches also act as a feedback loop to shift the rising and falling edges of sel1 and sel2 so they occur in line with the falling edge of pong (and thus the rising edge of ping).

The ping, pong, and reset-generating circuitry outside of the latches is another feedback loop controlled by capacitor C8 and nfet diff pair T38 and T40. When reset is low, pfet T94 is on and charges up the capacitor, which turns on T38, which pulls down and turns on pfet T113, which pulls up and turns on nfet T43, which pulls down. As a result, T40 turns off, but this also turns on pfet T115, which pulls up on the reset signal, switching it from low to high. When reset switches from low to high, pong is high and ping is low. The reset signal is high except for transition periods in the select signals, when it sharply plummets to a voltage level below the mid-point.

Figure 10: Schematic of BiCMOS 130nm Timer

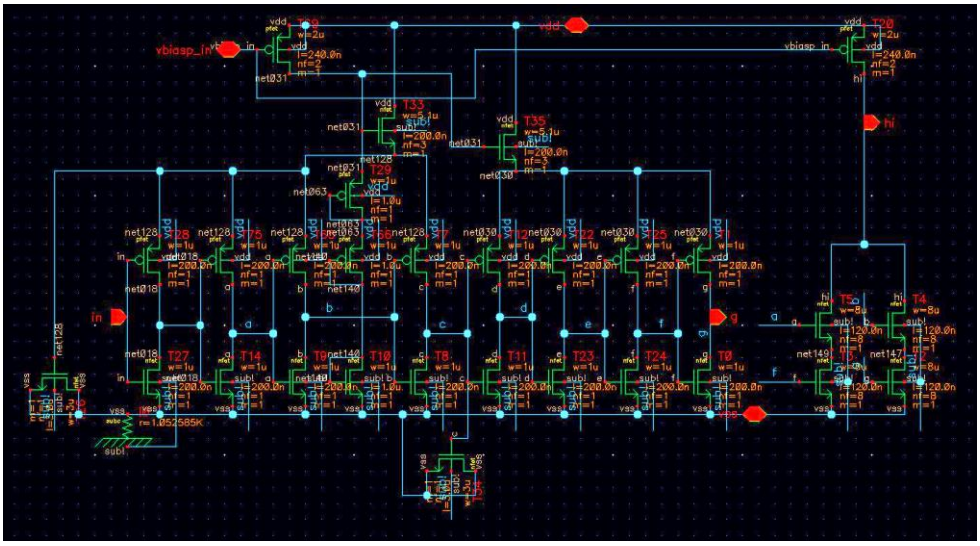


Pulsers

The two Pulsers are level shifter circuits. The stack of MOSFETs including diode-connected pfets T29 and T66 and diode-connected nfet T10 set the gate voltage of the two nfet current sources, T33 and T35, which limit the supply to both halves of the inverter chain (Figure 11). The chain of inverters provide minor delays, which control when signal “hi” is pulled down. Pulser 1 boosts the high-level or “on” amplitude of the digital signal (e.g.: from 467mV to 704mV, according to a simulation with 1mV 1kHz input sinusoid). This signal, called Pulseg in Figure 1, is the g output signal of Pulser 1, which becomes the in signal for Pulser 2. The hi signal from Pulser 2 is signal Cn, which is a high-level signal that pulls down during transitions

in the Digline signal and recovers with the resistor-capacitor-set time constant. Signal Cp functions in the same way, but pulls down during transitions in Pulseg.

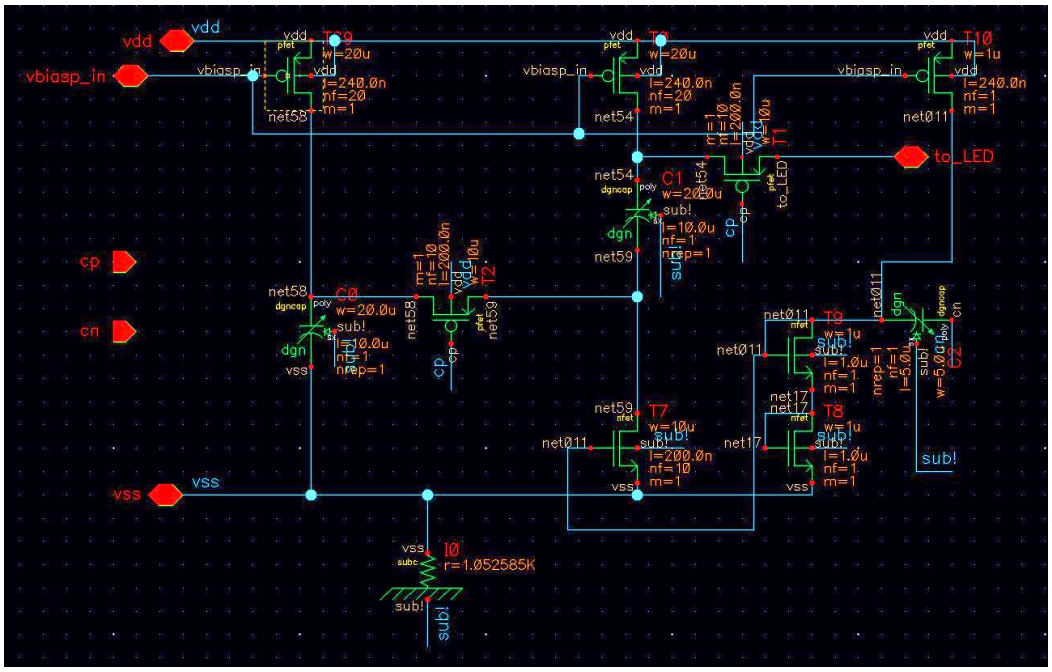
Figure 11: Schematic of BiCMOS 130nm Pulser



LED Driver

The LED Driver is a switched-capacitor circuit that consists of pfet switches, dual gate capacitors, pfet current mirrors, and an nfet voltage bias circuit (see Figure 12). When signal Cp is low, pfet switches T1 and T2 are closed, so capacitors C0 and C1 are stacked, and unload their charge as the output. When Cp is high, the switches are open, so the capacitors are charging up in parallel via the voltage biases. When Cn is low the nfets boost the DC level of the bottom plate of C1 so that voltage is higher than the voltage at the top of capacitor C2. The circuit at the lower right, the nfet voltage bias circuit, is necessary to boost the voltage at the bottom of the capacitor so that when the capacitors stack, the voltage is ‘dumped’ onto the output signal. Crowbar current is a concern for this circuit because both nfets and pfets are on during switching, so the circuit consumes more power than is necessary for circuit function.

Figure 12: Schematic of BiCMOS 130nm LED Driver



The LED output signal should look like high-valued current pulses (around 760µA, for 300µV 2kHz input signal in simulation). These pulses appear in pairs, which we will call pulse pairs. In a sequence of four pulses, the odd pulses will be one signal type and the even pulses will be the other type, where the two signal types are timing signal and encoding signal. We will call adjacent pulse pairs (in which the first pulse of the pair is a timing signal) wither a proximate pair or a distant pair depending on the time duration between them (see Figure 13).

Figure 13: Diagram of Pulse Pairs

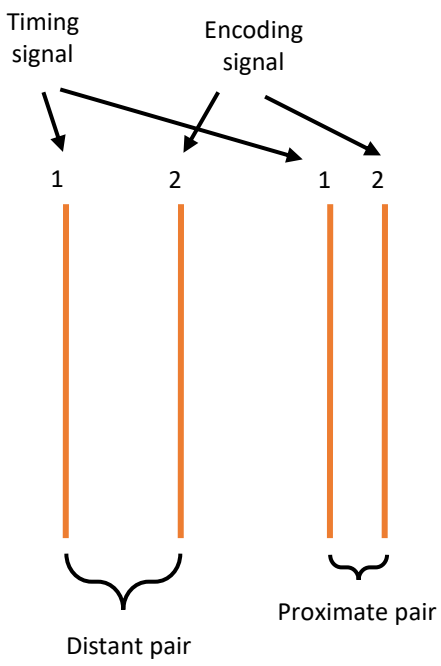
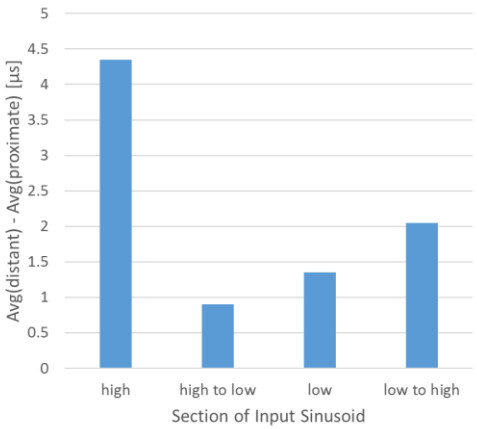


Figure 14: Difference Between Distant and Proximate Pairs for Section of Input Sinusoid



We simulated our MOTE under idealized test conditions (sinusoidal inputs of 500uV and 1mV at 1kHz for Vn and Vp) to find average durations between close and distal pulse pairs; this allowed us to determine patterns in the LED signal for different input signal valences. We determined that under ideal conditions, a peak in Vp (and therefore a trough in Vn) results in the largest difference between distant and proximate pairs, followed by a rising phase of Vp, a trough in Vp, and finally a high-to-low transition in Vp (see Figure 14).

Dynamic Range of MOTE Circuit

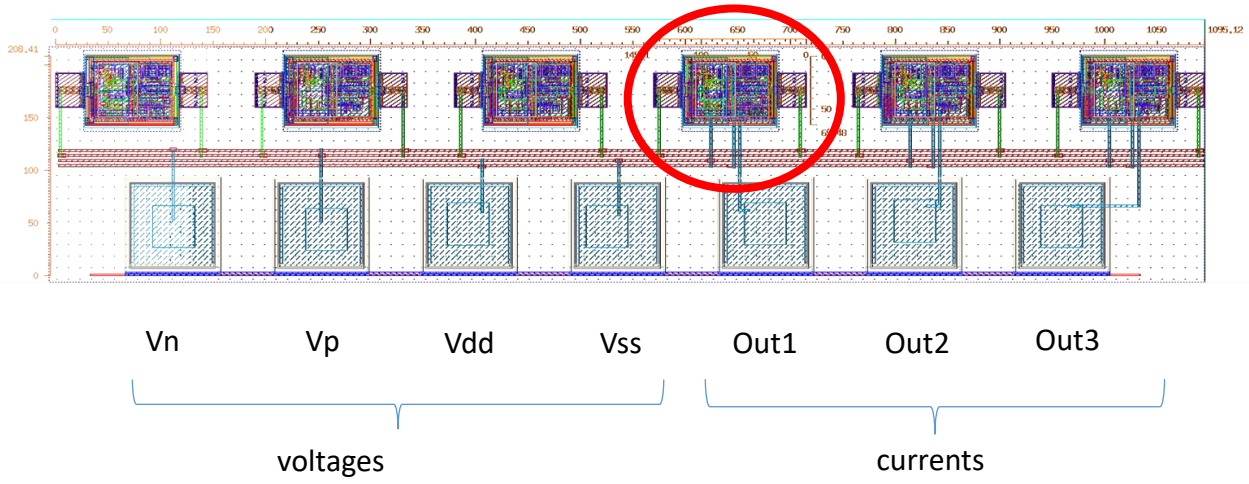
We tested the dynamic range of the MOTE circuits by varying the input amplitude of the sinusoidal neural input. With an input of 1mV amplitude and 1kHz frequency, we can easily distinguish the difference in LED output signal pulse pairs during peaks in Vp. When the amplitude is significantly increased or decreased, however, pulse pairs are disrupted. With a very low-amplitude signal such as 1µV, the difference in adjacent pulse pairs during Vp high is nearly

indistinguishable. For example, the difference between proximate and distant pairs was 100ns (proximate was 7.7µs and distant was 7.8µs) in one measurement. Conversely, with a large-amplitude signal such as 2mV, the pulse pairs during Vp low behave similarly to pulse pairs during Vp high in the ideal case, with obvious distinctions between proximate and distant pairs. During Vp high, the LED output signal is completely disrupted—pulse pairs appear to occur at half the expected frequency (21.7kHz instead of approximately 50kHz). We determined that the minimum timing for encoding a pulse pair is 5.04µs. Below this duration, the encoding pulse becomes two pulses in rapid succession or disappears. The dynamic range of the MOTE circuit is poor, as input amplitudes less than 1mV above or below 1mV cause disfunction.

130nm BiCMOS Layout

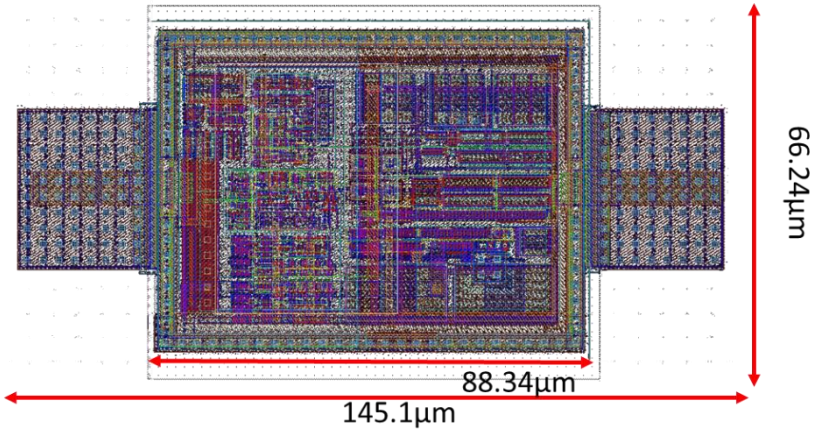
The 130nm chip we tested was the most complete version of six circuits that shared the same input, power, and ground pads (Figure 15).

Figure 15: Array of 130nm BiCMOS Circuits with Pads



We used the pad “Out1,” which corresponds to the output LED current signal from the indicated circuit. This circuit was smaller than the goal of 100µm^2 when the metal pads on the side are excluded (Figure 16).

Figure 16: Close-Up of Tested 130nm Circuit



However, the circuit is solely for laboratory testing, as the circuitry is incompatible with power and ground connections to GaAs LEDs.

CHAPTER 3

NEURAL MOTE IMPLANTS: 130NM BICMOS TESTING RESULTS AND CONCLUSIONS

PCB Problems and Solutions

We had to make several changes to the PCB circuitry and set-up due to human error in the PCB design. First, the op-amp used for parts U2 through U7 (see Figure 3a), surface-mount UA741, requires a supply voltage between 5V and 22V, however the IC cannot tolerate more than about 3V for Vdd, as the high power fries the chip. Our solution was to use two PCBs; one with only the IC (bonded to Spectrum Semiconductor's Sidebraze Dual In-Line Ceramic Package CSB02491), caps C1 and C2, and header pins connected, and the other with all op-amps, resistors, and caps connected. We used +6V and -6V for the latter and 1.5V and 0V as Vdd and Gnd, respectively, for the PCB with the IC.

Another major change was we had to change several connections on the PCB itself using a razor blade and soldering. Since outputs 1, 2, and 3 each connected to a complete version of the MOTE, we narrowed our focus to outputs 1 and 2, corresponding to op-amps U2 and U3. Pads 3 and 7 of U2 and U3 were incorrectly connected to ground in the PCB design. So, we had to scratch out the copper fill that made those connections. Additionally, we had to scrape around pad 3 and cut the connection between pad 3 and the header pin to ensure there were no shorts to ground. We removed all solder connecting pin 3 of the op-amp to pad 3 on the board, just in case. We soldered wires to pin 3 of U2 and U3, and connected these to a Keithley DC voltage source set at 1.5V. This serves as the bias voltage for the transimpedance amps.

A final PCB issue was the resistor and capacitor sizing for these amplifiers. The resistors were originally set at 1kOhm, and the capacitors to 5pF. According to the datasheet for UA741, the typical gain-bandwidth product is 1MHz. Therefore, according to Equation 6, the signal

through the amplifier would actually be degraded (A1*A2 = 0.005). Thus, we needed to determine appropriate resistor and capacitor values for productive output signal amplification. The voltage buffers (unity gain buffers) on the PCB (U5, U6, and U7) were not able to support the gain we were looking for, so we did not use them in the set-up.

Testing Results

Initial testing of our 130nm chip proved several successes despite poor resolution with the first set-up. First, the circuit consumes little power—between 3μm and 4μm for all four chips tested. Additionally, we detected some periodicity in that some noisiness in the oscilloscope appeared to be the encoding spikes moving left and right. However, we believed that much of what we were seeing on the oscilloscope was 60Hz noise (AC current due to electricity in the testing room). We needed faster processing, so we set up the NI DAQ (both the oscilloscope and the DAQ have 10ns timing resolution, but the DAQ is less noisy and allows for easy MATLAB data analysis).

We attempted several filtering fixes using a breadboard. We added a notch filter to the LED output signal in an attempt to dispel both the ringing we saw after each output spike and the 60Hz noise. However, this method did not work, and actually changed the output into a sinusoid. To solve our output signal problems, we added a low-pass filter on the breadboard, and created an on-PCB filter by re-soldering the transimpedance amplifier's capacitor in parallel to its feedback resistor. We also calculated that the sinusoidal input signal was degraded from 40mV in the function generator to 33mV in the DAQ, so we had to calculate new resistor combinations on our breadboard to account for this while also reducing the function generator output to the appropriate levels for the input signal. (The smallest signal that the function generator can produce is 40mV peak-to-peak, but we want input signals between 100μV to 1mV.)

Our code connects the Dell computer to the NI DAQ system, filters noise, and thresholds data (see Appendix 2). The DAQ PXIe card does not consistently assign a particular channel to

an input on the SCB, so we add to re-add the analog input channels for each test iteration. We set a voltage range for each channel (Vp input and LED output signal), data acquisition rate (2 million samples per second, the maximum for the chassis used), and sampling duration.

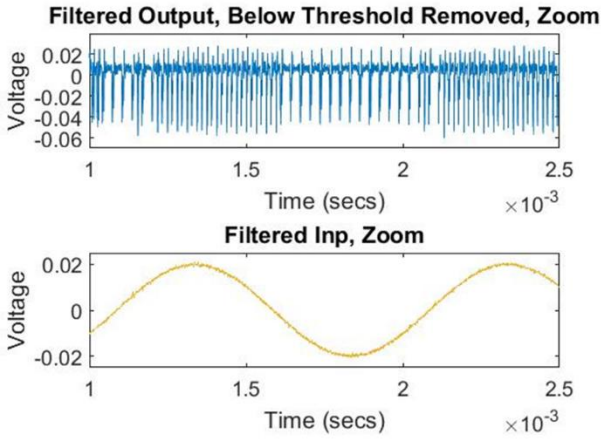
We located and filtered noise in the output LED signal by finding the discrete Fourier transform of our data (8000 samples for both channels) to determine the frequency components of our data. Then, we plotted the data with a log scale for the y axis (voltage), looked for the peaks, and zeroed out the matrix for those frequencies (and for the first row to make the DC term 0). We took the inverse Fourier transform of this new matrix, and then isolated the real components, creating a low-pass-filtered version of the original data. After filtering, we thresholded the output data by determining a value that is higher than the small, noisy jitter but below the smallest spikes. We set data points below the threshold to zero. This provided data that often resembled our expectations for the output spikes.

We also wrote MATLAB code to search for optimal timing pulse widths because we saw that the initial tests did not demonstrate distinct proximate and distant pairs (see Appendix 3). We determined that a period of timing pulses should contain 40 to 60 samples, and set an arbitrary pulse width (in number of samples). Then, we created an idealized pulse train with which we convolved the output data set, and took the Fourier transform to find a peak in the frequency data where the pulse train and data overlap often. This represents an optimal timing pulse period, so we repeated the convolution with that number (instead of looping for 40 to 60). We used this convolution to determine how many zeros to add to the beginning of our fabricated pulse train in order to achieve maximum overlap. This methodology did not work well for all of the data sets, and it is probably due to lack of robustness in our MOTE chip, noise in our testing set-up, or the fact that there should be more than one pattern of pulse trains depending on the stage of the input voltage (Figure 13).

The data we collected using the NI DAQ showed that 500μV peak-to-peak input signals resulted in the best output data, and 1kHz was the best frequency. We collected data for inputs between 100μV and 30mV, and frequencies between 300Hz and 10kHz. For the 100μV signals

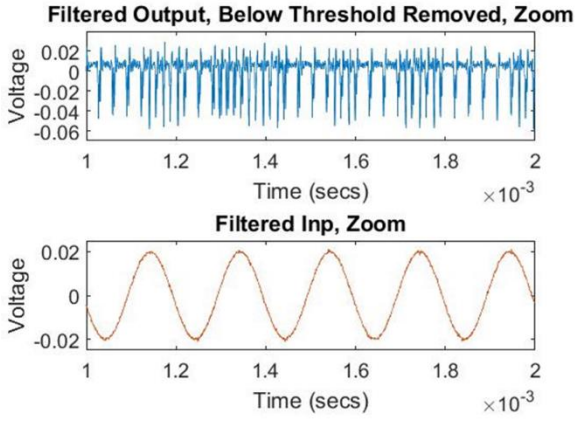
at 1kHz, the timing signal period was 32µs and encoding signals appear to form during Vp high, but they are absent during Vp low (Figure 17).

Figure 17: Vp Signal (100µV 1kHz) and MATLAB-Processed Output LED Signal



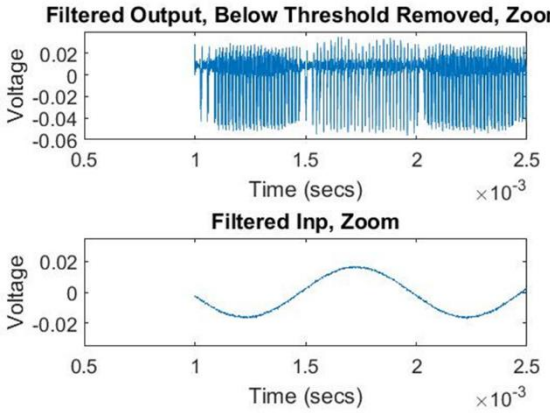
However, higher or lower frequency inputs completely degrade the output signal, as in Figure 18, wherein it is unclear which signals are timing or encoding, and which signals have dropped out.

Figure 18: Vp Signal (100µV 5kHz) and MATLAB-Processed Output LED Signal



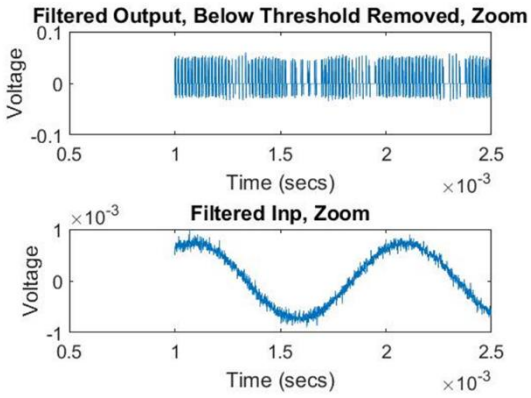
500µV input signals at 1kHz provided consistent, if still unexpected, results with respect to time between pulses and regular presence of encoding signals during both Vp high and Vp low (with the exception of a short period at the middle of each transition from high to low, Figure 19).

Figure 19: Vp Signal (500µV 1kHz) and MATLAB-Processed Output LED Signal



During Vp low, time between timing and encoding pulses was approximately 15µs, while time between timing and encoding pulses during Vp high was approximately 31µs. 1mV 1kHz input signals gave similar results as 500µV at 1kHz, but with more frequent encoding pulse skipping (Figure 20).

Figure 20: Vp Signal (1mV 1kHz) and MATLAB-Processed Output LED Signal



Higher-amplitude input signals resulted in uninterpretable LED output signals.

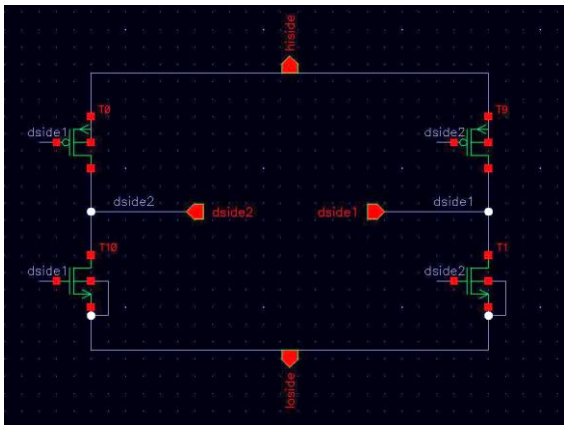
CHAPTER 4

NEURAL MOTE IMPLANTS: 180NM CIRCUITRY

Polarizer

The Polarizer determines which side of the GaAs is high, and which side is low, based on voltage level. If the voltage level of the LED pad connected to Dside1 is high, pfet T0 will be off but nfet T10 will be on. Thus, the Dside2 pin will be pulled toward "loside" (Figure 21). Furthermore, when Dside1 is high, Dside2 will be low in comparison, so pfet T9 will be on, nfet T1 will be off, and Dside1 will be pulled toward "hiside" (and vice-versa for the case wherein Dside2 is high). Thus, the higher-voltage side of the GaAs LED will be assigned to the correct pins within the circuit.

Figure 21: Schematic of 180nm Polarizer

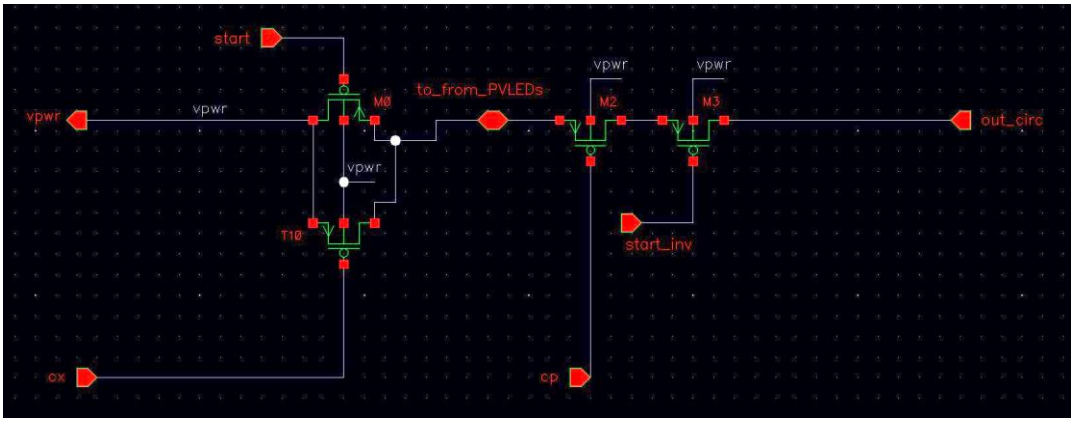


Share PV

This circuit controls whether the GaAs LED functions as an LED that flashes an output pulse or as a power source for the whole circuit (via Vpwr) (Figure 22). At the startup stage of the circuit, the Start signal is low, so pfet switch M0 is on, and the high side of the LED acts as a photovoltaic, pulling up Vpwr. From then on, the LED powers the circuit whenever Cx is low.

When Cp is low (after Startinv's transition from high to low), the LED output current signal of the circuit passes through to the high side of the LED, prompting photon emission.

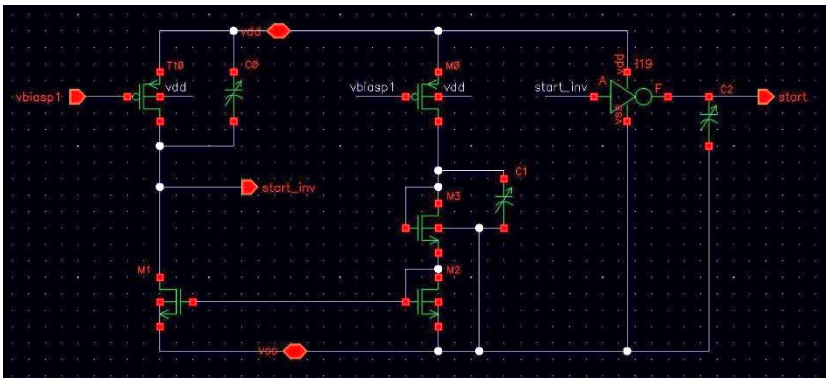
Figure 22: Schematic of 180nm Share PV



Share PV Startup

This circuit serves as a startup pre-circuit for the Share PV circuit (Figure 23). We assume that the Vbiasp1Start signal from the PTAT is initially low because the Vpwr signal is initially low in any given test scenario. In the left branch of this circuit, Startinv is initially high because pfet T10 is on and is pulling up. Capacitor C0 provides a time constant to the pull-down effect as Vbiasp1Start goes high. In the middle branch of the circuit, capacitor C1 charges up initially while the pfet switch M0 is on. Then, when Vbiasp1Start is high, C1 discharges through the nfet stack, providing a time constant to the nfets' pull-down effect. The inverter outputs the Start signal and capacitor C2 gives a time constant to the switching of Start from low to high.

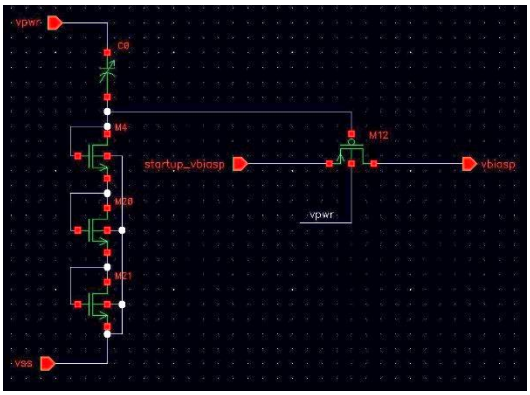
Figure 23: Schematic of 180nm Share PV Startup



Startup Switches

The two Startup Switches initiate basic function of all active circuits after startup of the PTAT circuit. The signal controlling the pfet switch M12 is initially high, but as the capacitor charges up, the signal is pulled down and that is when Startup Switches 1 and 2 connect the PTAT Vbiasp signals to the other functional sub-circuits (Figure 24).

Figure 24: Schematic of 180nm Share PV Startup Switches



Driver Switch Controller

The Cp signal from Pulser 2 controls Cx, the output signal of the Driver Switch Controller. When Cp is high (most of the time), Cx is weakly pulled down by nfet M1 since pfet T0 is open. When Cp is low, however, Cx is pulled high (Figure 25).

Figure 25: Schematic of 180nm Driver Switch Controller

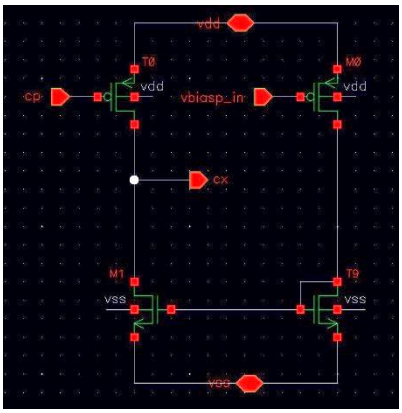
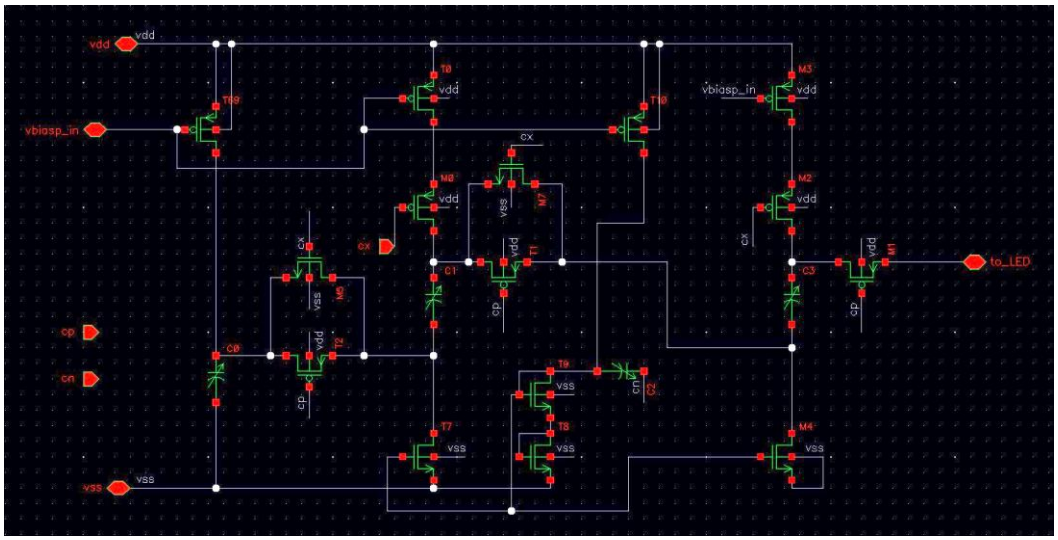


Figure 26: Schematic of 180nm LED Driver



The Cx signal minimized crowbar current in the LED Driver circuit by ensuring clean transitions between charging and stacking states of the switched capacitors (Figure 26).

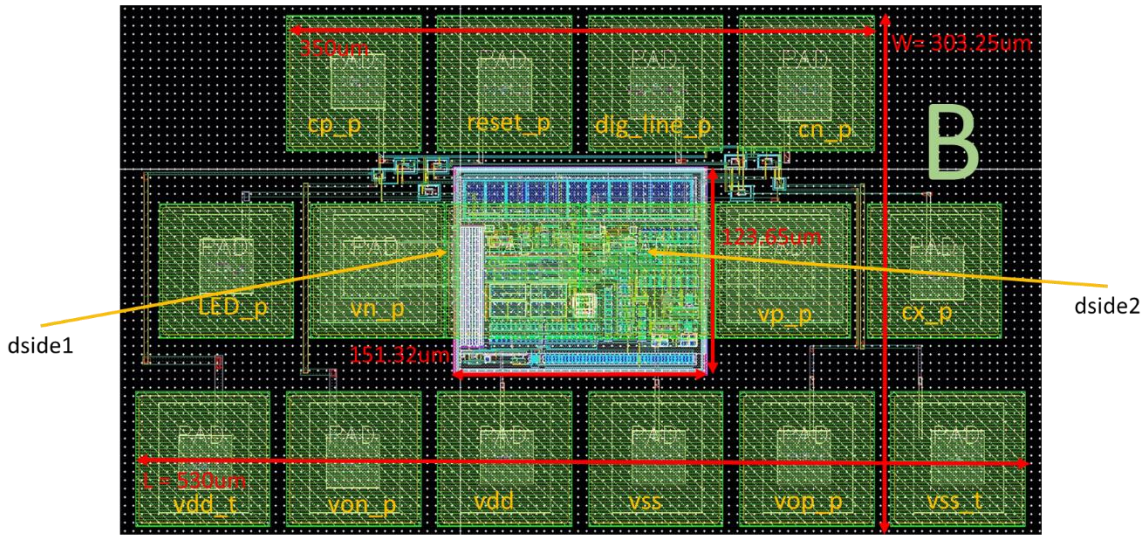
CHAPTER 5

NEURAL MOTE IMPLANTS: 180NM TESTING RESULTS AND CONCLUSIONS

180nm Layout

The 180nm IC basic layout enables connection to GaAs LEDs via direct contact/flip-chip bonding or using wirebonds, however normal circuit testing is challenging, so we created a break-out version of the circuit which allows for off-chip power and ground supplies (Figure 27).

Figure 27: 180nm IC Layout—Breakout Version



This version includes a doublet in the OTA amplifier for increased input voltage linearity (although maximum linearity would have been achieved had the doublet been attached in the Encoder amplification stage), and three capacitors in the LED Driver circuit.

Our non-breakout versions include the 2-LED Cap layout (Figure 28), the Doublet 3-LED Cap layout (Figure 29), and the Doublet 3-LED Cap Updates layout (which is very similar to the Doublet 3-LED Cap version except it includes larger capacitors, the Driver Switch Controller sub-circuit, and the nfet switches within the LED Driver circuit, Figure 30).

Figure 28: 180nm IC Layout—2-LED Cap Version

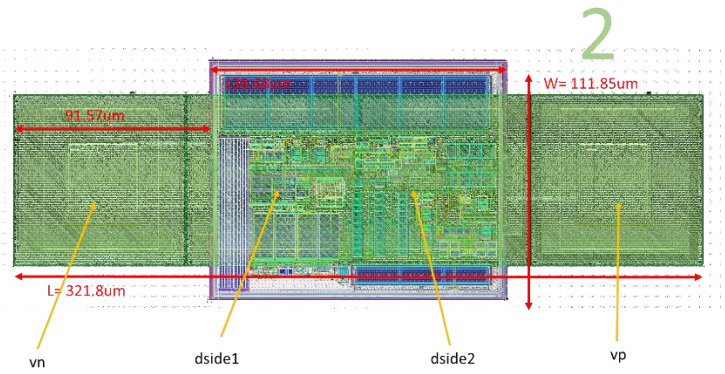


Figure 29: 180nm IC Layout—Doublet 3-LED Cap Version

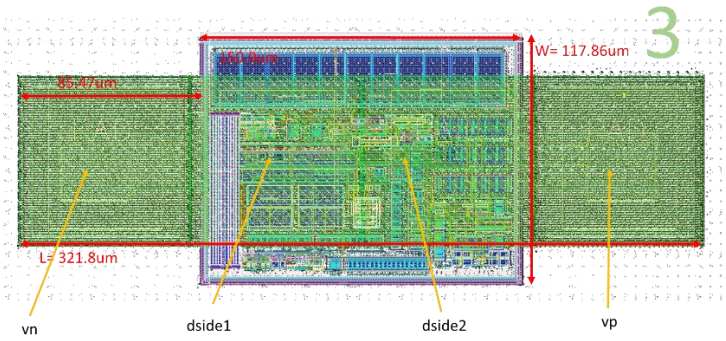
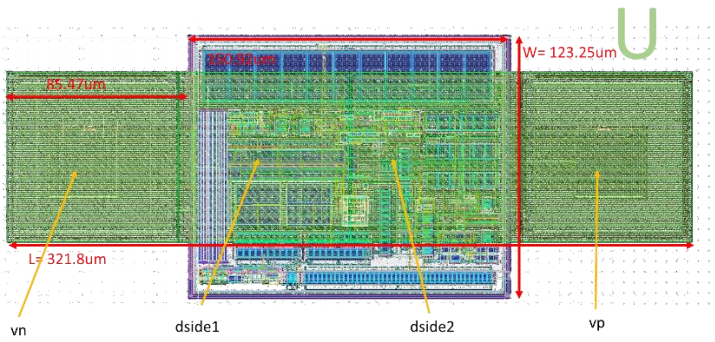
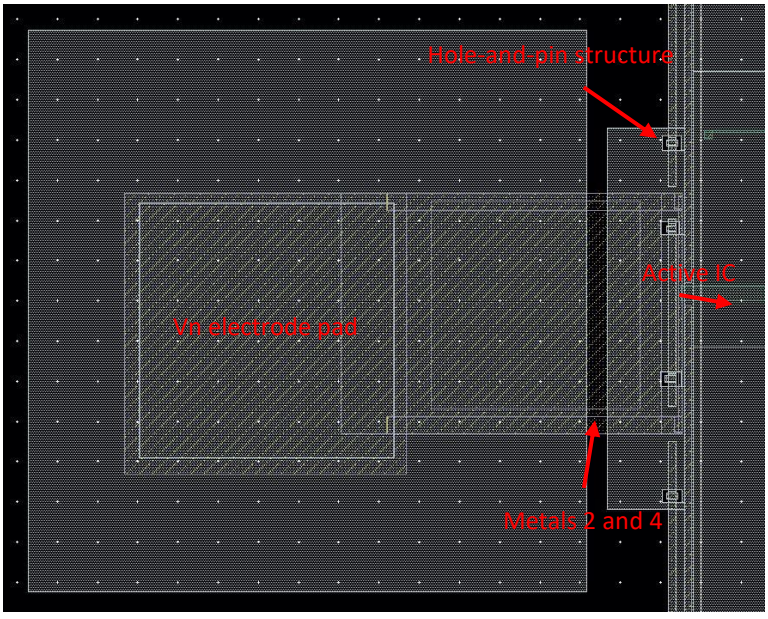


Figure 30: 180nm IC Layout—Doublet 3-LED Cap Updates Version



The functional circuits in all of these layouts are enclosed by specialized guard rings, which separate Vpwr from Vss, and isolates these from other signals. The outer guard ring is a connection between the psub layer and Vss, and the inner guard ring is a connection between the nwell layer and Vpwr. Additionally, all of these layouts include metal pads that will function both as pads for input signals Vp and Vn as well as electrodes to pick up the neural signal. We constructed these pads from all of the even-numbered metal layers (M2, M4, M6), and created the two central pads (Dside1 and Dside2) using M6. Since we wanted a strong mechanical connection between the electrode pads and the rest of the IC, we developed a hole-and-pin structure on the left and right sides of the guard ring (Figure 31). This allowed us to create a bridge out of thick bands of the even-layer metals between the electrode pads and the main IC.

Figure 31: Close-Up View of Doublet 3-LED Cap Updates Demonstrating Mechanical Connections

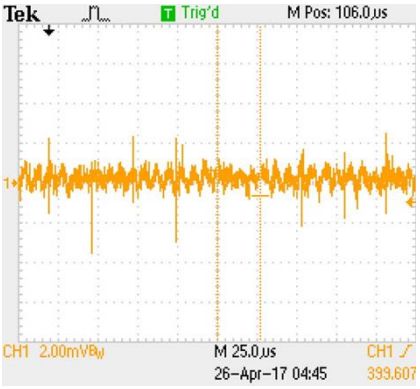


Note that only M2, M3, M4, and M5 are visible in this image for clarity.

Basic Functionality Testing

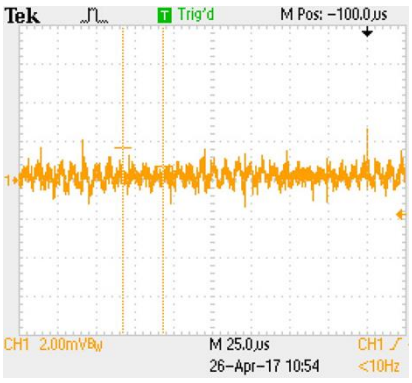
We tried four tests on the Doublet 3-LED Cap Updates version, and verified basic functionality of the circuitry. For all of these tests, we wirebonded the four pads to a Side-Brazed Dual In-Line Ceramic Package, and placed that package in a breadboard. For the first test, we attached the Dside2 pin of the package to the ground of the function generator, and allowed Dside1 to float (Figure 32). Then, we reversed the direction of the ground node, allowing Dside2 to float (Figure 33).

Figure 32: Oscilloscope-Measured Signal from Dside1



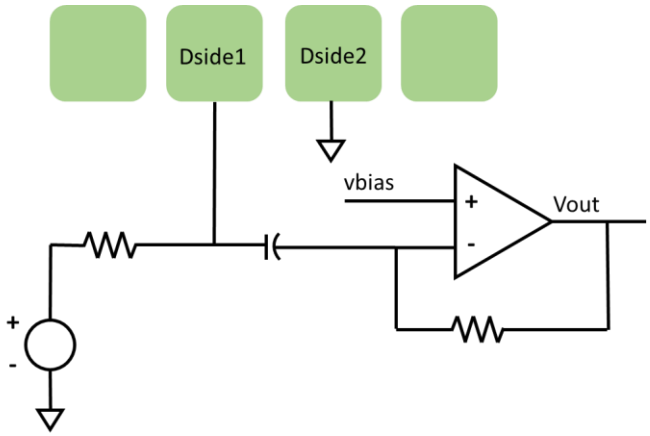
In this test, Dside1 was allowed to float while Dside2 was grounded.

Figure 33: Oscilloscope-Measured Signal from Dside2



In this test, Dside2 was allowed to float while Dside1 was grounded.

Figure 34: Signal Separating Circuit for 180nm Chips



In both set-ups, the chip generated a slight voltage difference with a periodic spiking pattern at 38.5kHz (a period of 26µs). This result indicates that some oscillatory function—probably generated by the Timer circuit—functions, as well as start-up circuitry—particularly the Polarizer, as switching the polarity of the LED input pads seemed to have no effect on the output from the floating pad. Unfortunately, tests that connected the IC to an off-chip signal-separating circuit did not show any signs of spiking oscillation (Figure 34).

CHAPTER 6

BIOCOMPATIBLE PACKAGING

Overview of Project

ICs with 3D time-resolved imaging capabilities can image microorganisms and other biological samples given proper packaging. A portable, flat, easily manufactured package will enable users to place biological samples on slides directly above the imaging chip. We have developed a packaging procedure for our group's imager IC chip using laser cutting, photolithography, epoxies, and metal deposition. In the Cornell Nanoscale Science & Technology Facility (CNF), we have finalized this packaging procedure after experimentation with a flip-chip method, and we have aligned and adhered the chip to a holder wafer.

We first attempted a flip-chip strategy incorporating a patterned fused silica wafer as a combination biological sample slide and connection between the imager chip and a printed circuit board (PCB). Flip-chip machines such as the Finetech FINEPLACER Lambda use vacuum chucks and micro-positioners to align bond-pads on a chip to another device. Researchers can pattern solder or gold ball bumps onto bond-pads and heat to cure after performing the flip-chip process. We unsuccessfully attempted flip-chip using anisotropically conductive adhesive (Creative Materials Anisotropic Conductive Thermoplastic Adhesive 111-05) to electrically and mechanically bond the imager chip to the patterned fused silica wafer (11).

Gold Breakout Chip Fabrication

After designing a pattern for a photomask to create metal connection lines between the chip's bond-pads and a PCB, we patterned the mask using the Heidelberg Mask Writer DWL2000. We spun LOR10A and SPR220 photoresist (PR) onto fused silica wafers, exposed

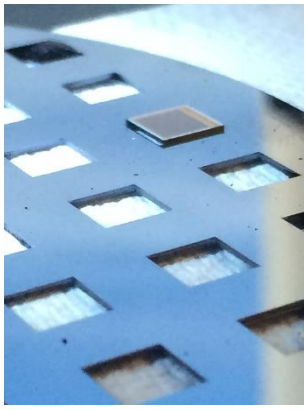
them with the mask, and developed them. We then evaporated titanium (adhesion layer), copper, and gold onto the wafers, and then performed lift-off and diced the wafers. Our preliminary tests bonding the patterned wafer pieces to the chip using 111-05 did not result in electronic connections.

Silicon Packaging for Best Fit

After moving on to a flat package concept, we sought to minimize the inevitable gap between the imager chip and its holder wafer. We designed a pattern for the mask with a gradient of squares (minimum size $5mm^2$, the size of the imager chip), which at the end of the process became cavities to find the best fit for the chip. We used the Oxford 100 Plasma Enhanced Chemical Vapor Deposition System (PECVD) to deposit 4um of SiO_2 (oxide) on the top of the Si wafer and 1µm on the bottom. The thick oxide on top serves to protect non-cavity areas of the wafer from the Si etch, and the thinner oxide on the bottom serves as a Si etch-stop.

We then spun SPR220-4.5 PR on the wafer, exposed with the cavity gradient mask, and developed. Then, the Oxford 82 was used to etch through all of the oxide in the square cavity areas. We used a CHF_3 etch process (etches oxide at approximately 35nm/minute) until only 100nm remained on the cavity areas, and then we switched to a CF_4 etch process (etches oxide at approximately 31nm/min) because unlike CHF_3, CF_4 does not deposit unwanted polymer after etching all the way through the oxide. We subsequently used the Unaxis 770 Deep Si Etcher to etch through Si to form the square cavities in the Si wafer. The tool etches Si at around 2µm/min and 1µm oxide for every 150µm Si. Finally, we removed the 1um etch-stop layer of oxide by submerging the wafer in pure HF. Unfortunately, even the largest cavities ($5080\mu m^2$) were too small for the imager chips (Figure 35).

Figure 35: Microscopic view of 5mm^2 chip on top of cavity gradient wafer



Imager Chip Alignment and Adhesion

After discussion with CNF staff, we decided to explore a process using one purposefully over-sized cavity in the center of a Si wafer because we figured a larger gap could be easier to fill with adhesive. We used three wafers in this process: a Si holder wafer with a square 6.5mm^2 cavity, a fused silica handle wafer to help align the top of the handle wafer with the top of the chip, and a fused silica carrier wafer to push the adhesive into the gap between the holder and the chip (Figure 36).

Figure 36: Diagram of Entire Package—

Holder Wafer, Imager Chip, Handle Wafer,

Carrier Wafer

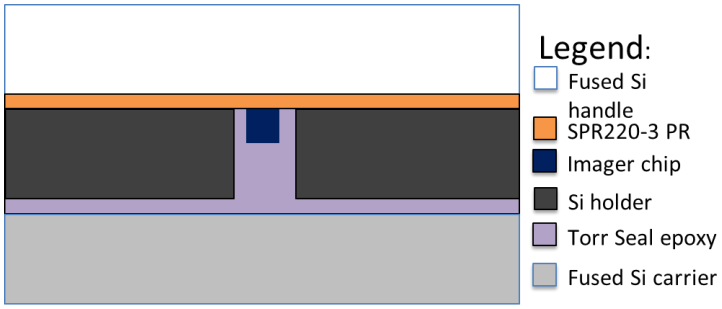


Figure 37: Planarized Chip in Holder Wafer

We used the Lal group's LPKF ProtoLaser U tool to cut a 6.5mm^2 hole in a Si wafer (holder wafer). Then, we spun SPR220-3 on a fused silica wafer (handle wafer), placed the holder wafer and the chip top-down onto the handle wafer, and baked the package to bind the pieces together. Outside of the CNF, we prepared Varian Torr Seal adhesive and applied it to the fused silica carrier wafer, then pressed the adhesive side onto the backside of the package (backside of the chip and holder wafer) (12). After curing at room temperature for 24 hours, we soaked the package overnight to remove the handle wafer and PR. The top surfaces of the holder and the chip were sufficiently co-planar for our needs: the top of the chip is 8.7µm above the holder wafer, with the Torr Seal protruding 10.2µm above the holder wafer surface and 1.5µm above the chip surface (Figure 37).

CHAPTER 7

FABRICATED CAPACITORS

Project Overview

Further research has been performed on a long-term metal-insulator-metal (MIM) capacitor characterization project. Former CNF Fellow and continuing CNF User Kwame Amponsah developed the original procedure for the capacitor fabrication, and another former fellow, Jonilyn Longenecker, revised the procedure and began the arduous process of characterization. MIM caps are useful to clean room users as testing devices to verify electronic characteristics of their active circuitry. This project's objective is to determine differences in current-voltage (IV) and capacitor-voltage (CV) relationships across variations in capacitor size and dielectric type. This effort requires an approximately 20-step process repeated for two-to-six varieties (dependent on temperature and thermal versus plasma options) of the following dielectrics: HfO2, SiO2, Al2O3, TaOx, and TiO2. See Appendix 3 (**not located yet**).

Improvements to Original Procedure

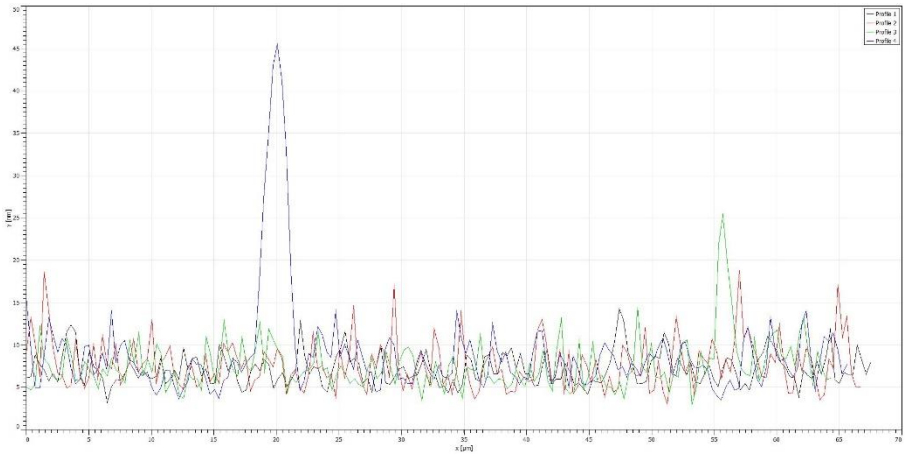
The first procedural problem is Part 1, step 1(a), spinning LOR10A resist. This photoresist is extremely thick, which is excellent for clean lift-off procedures. Its viscosity, however, creates streaking when spinning at high accelerations, resulting in uneven application. To solve this problem, we decreased the rpm for the first stage and rpm/sec for both stages of the spin. The first stage is now 250 rpm at 250 rpm/sec for 2 seconds, and the second is now 3000rpm at 1000rpm/sec for 45 seconds. This method significantly improved evenness on the

wafer, but the edges were still streaked with the resist, so we pour directly from the bottle in a spherical pool, and then the first stage of the spin provides a smooth, even coating.

We have also revised Part 1, Step 7, the evaporation step. First, we encourage other people performing this procedure to attach wafer pieces to the evaporation stage using Kapton tape (polyimide heat resistant tape) instead of the screw-in metal clamps because of improved ease of use and less damage to the pieces. For Part 4, the repetition of Part 1 for the second metal layer, this improvement is especially helpful since each piece will be one-sixteenth of a wafer (each piece is a quarter of a wafer during Part 1).

Additionally, we discovered via atomic force microscopy (AFM) that the platinum layer of the evaporation step is prone to undesired spikes or peaks, possibly due to spitting (Figure 38). Spitting occurs when a platinum source crucible ejects platinum sporadically when exposed to high power. For the metal evaporation in Part 1, we now deposit an extra 50nm chromium layer after the platinum layer to cover any spikes. We hypothesize that spikes in the platinum layer of Part 1 contributed to poor adhesion of the ALD layer and thus the second metal later as well. We will ensure a pristine surface for Part 2, ALD film deposition, by soaking the pieces in BOE (buffered oxide etch, a solution of HF acid) for twenty seconds, rinsing with DI (deionized water, provided throughout clean room), and then dehydrating them for a minute on a 150C hot plate immediately prior to the deposition.

Figure 38: Profiles of Four Scans of 90µm^2 Area of Pad



This image shows the 3D profile of four scans across a 90µm^2 area of a Cr-Pt pad captured via AFM. These profiles were measured using the Gwyddion scanning probe microscopy imaging software.

We made some minor changes to the procedure in addition to the above revisions. We also added another alternate step for Part 1, step 6, the descum step. Cleaning the wafer pieces in the Anatech Resist Strip plasma etcher for one or two minutes gives a similar result as the Oxford 82 and Aura 1000 procedures provided. Additionally, we bumped the recommended 5nm chrome adhesion layer (first evaporation step for Parts 1 and 4) up to 15nm. For Part 1, step 8, we increased part (a) to 10 minutes, and increased part (b) to 20 minutes. For Part 4, step 6, there is no need to descum in the Oxford 82 unless the ALD layer is Al_2O_3, in which case one should perform a 90-second ARC (AR3) etch. Finally, we added a note to prepare a bath of DI water in which to stop the etch in Part 5.

APPENDIX 1: Subthreshold Equations for MOSFETs

Subthreshold Current Equations:

$$V_G < V_{th}$$

Pfet: $$I_D = I_{0p}\frac{W}{L}exp\left(\frac{\kappa(V_W - V_G)}{U_T}\right) \times \left[exp\left(\frac{-(V_W - V_S)}{U_T}\right) - exp\left(\frac{-(V_W - V_D)}{U_T}\right)\right]$$

Nfet: $$I_D = I_{0n}\frac{W}{L}exp\left(\frac{\kappa V_G}{U_T}\right) \times \left[exp\left(\frac{-V_S}{U_T}\right) - exp\left(\frac{-V_D}{U_T}\right)\right]$$

Nfet, simplified: $$I_D = I_{0n}\frac{W}{L}exp\left(\frac{\kappa V_G - V_S}{U_T}\right) \times \left[1 - exp\left(\frac{-V_{DS}}{U_T}\right)\right]$$

Subthreshold Saturation Current Equations:

Pfet:

$$|V_{DS}| > 4U_T$$

$$I_D = I_{0p}\frac{W}{L}exp\left(\frac{\kappa(V_W - V_G) - (V_W - V_S)}{U_T}\right)$$

Nfet:

$$V_{DS} > 4U_T$$

$$I_D = I_{0n}\frac{W}{L}exp\left(\frac{\kappa V_G - V_S}{U_T}\right)$$

In the following equation for Nfets in subthreshold saturation, the distributed kappa is incorrect, however this error allows us to simplify the power-size trade-off as seen in Equation 5.

Citation for these equations:

Harrison, Reid R. "The MOS Transistor in Weak Inversion." *MOSFET Operation in Weak and Moderate Inversion*. University of Utah.

APPENDIX 2: MATLAB Signal Processing for 130nm Testing Using DAQ

Primary code: Test130nm 2.m

```
clc; close all; clear all;

% Connect to DAQ, Set Up Session

% devices = daq.getDevices;
% %devices(1) %print the properties of the PXIe subsystems
s = daq.createSession('ni');
ch1 = addAnalogInputChannel(s,'PXI1Slot2', 9, 'Voltage'); %output1 of chip is
on channel 9
ch2 = addAnalogInputChannel(s,'PXI1Slot2', 10, 'Voltage'); %inp of chip is on
channel 10
ch1.Range =[-5 5]; %sets voltage range -5V to 5V (default is -10V to 10V),
signal disappears if try [-1 1]
ch2.Range =[-1 1]; %sets voltage range -1V to 1V (default is -10V to 10V),
least pixellated option
s.Rate = 2000000;%max daq rate for this PXIe
s.DurationInSeconds = .004;%duration of data capture. For 1kHz, 4 pds is 4ms,
and at 2MS/s, that means first 8k samples of the matrix
% s %print the properties of the current session
[data,time] = s.startForeground;%collect data


% Plot Data

figure(1)
set(gca,'fontsize',14)
hold on
xlabel('Time (secs)');
ylabel('Voltage');
title('Inp and Output');
plot(time,data(:,1)-ones(size(time))*(mean(data(:,1))+0.0073)) %plots time on
x-axis, both columns of data adjusted to remove DC offsets
plot(time,data(:,2)-ones(size(time))*(mean(data(:,2))))
%ones is a vector the size of the time vector, and it's populated by the
%mean of the respective data vector
hold off

% Locate and Filter Noise
figure(2)
L = length(time);
Fs = 2000000*(1:L);
%find discrete Fourier transform of data matrix
burt=fft(data);
semilogy(Fs,abs(burt));
%plots y axis data (data matrix) using the log
% scale, fft used to find frequency components of noisy signal
%look at the peaks, and determine which relates to noise

burt(4000:7000,:)=0; %zero out the matrix for indices that include the noisy
frequencies
```

```
burt(1,:)=0; %zero out first row of burt
ernie=ifft(burt); %take inverse Fourier transform of burt

figure(3)
hold on
plot(abs(ernie(:,1)))
set(gca,'fontsize',14)
xlabel('Time (secs)');
ylabel('Voltage');
title('Filtered Inp and Output');
hold off

%plot(real(ernie)) %plots improved signal by index
data_f = real(ernie);
figure(4)
xlabel('Time (secs)');
ylabel('Voltage');
title('Filtered Inp and Output');
subplot(2,1,1), plot(time,data_f(:,1))
subplot(2,1,2), plot(time,data_f(:,2))
% plot(time,data_f)
% hold off

% Thresholding

threshold  = 0.02; % set a threshold was .004 then .02
data_f2 = data_f;
% data_f2 = data_f2-ones(size(time))*0.0065;%new
data_f2 = data_f2*[-1; 1]; %mirror over x-axis since the transimpedance
% amp is inverting
% data_f2(:,1) = data_f2(:,1)*-1;
data_f2((abs(data_f2(:,1)) < threshold), 1) = 0;
figure(5)
set(gca,'fontsize',14)
hold on
xlabel('Time (secs)');
ylabel('Voltage');
title('Filtered Inp and Output, Below Threshold Removed');
% plot(time,data_f2)
subplot(2,1,1), plot(time,data_f2(:,1))
subplot(2,1,2), plot(time,data_f(:,2))
hold off

% Zoomed-in view to see pattern

outplot = data_f2(2000:4999);%was 2000:4999   do 3999 for 5kHz
inplot = data_f(:,2);
% inplot = data(:,2);
inplot = inplot(2000:4999);
timeplot = time(2000:4999);%

figure(6)
hold on
% plot(time,data_f2)
subplot(2,1,1), plot(timeplot,outplot)
```

```
axis([1e-3 2.5e-3 -0.07 0.07])%y was -.04 to .06 %x was 0.5e-3 2.5e-3
title('Filtered Output, Below Threshold Removed, Zoom');
set(gca,'fontsize',14)
xlabel('Time (secs)');
ylabel('Voltage');

subplot(2,1,2), plot(timeplot,inplot)
axis([1e-3 2.5e-3 -0.025 0.025])%y was -1e-3 1e-3 %x was 0.5e-3 2.5e-3
title('Filtered Inp, Zoom');
set(gca,'fontsize',14)
xlabel('Time (secs)');
ylabel('Voltage');
hold off

% plot(time(1:4000,:),data(1:4000,:))
% plot(data(1:4000)-1.5)
% removeChannel(s,2); %removes an added analog channel (sometimes the
% output channel has moved from 9 to 4...)
```

More code: things.m

```
close all;

% this section of code looks for an optimal timing pulse width
% convolve signal with pulse train of different widths
% fft of result should have some kind of high peak

% for i = number of samples between timing pulses
for i = 10:100 %was 40:60
    p1 = zeros(1,i);
    % Arbitrarily chose pulsewidth to be 7
    p1(1:7) = 0.01;

    % repmat takes a short vector and copies it over and over
    % into a longer vector
    ptrain = repmat(p1,[1 160]);

    test = conv(data_f2(:,1),ptrain);
    figure(1)
    plot(test); hold on;
    figure(2)
    plot(abs(fft(test))); hold on;
end

%%
% choose a width that seems to be optimal and put it in here (sub for 56)
p1 = zeros(1,21); %was 56, then 86
p1(1:3) = 0.01; %was 1:5

repeat = 8000/25; %new: determine how many times to repeat the timing pulse
repeat = ceil(repeat); %round up to next integer
```

```
ptrain = repmat(p1,[1 repeat]); %repeat was 160

test = conv(data_f2(:,1),ptrain);
figure(3)
plot(test); hold on;

% % shift of some value based on looking at convolution.
% find sample is 8000. we expect maximum here
% but it's probably a little bit after.  Shift by that much.

ptrain = [zeros(1,3) ptrain]; %was 16 instd of 3

%%
figure(4)
plot(data_f2); hold on;
plot(ptrain)
```

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